Final Project Review

Supplemental Documentation

ECE3663 - Digital Integrated Circuit

Leiqing Cai (lc9ac)

Qing Qin (qq3za)

Ashley Morse (alm3tw)

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Simulation – Basic Features

The purpose of this simulation is to verify the delay metrics. Simulation was conducted under worst-case for the entire circuit, which is $A = 0x7FFF$, $B = 0x0000 \rightarrow 0x0001$. Function selected is addition, namely $s = 0b100$. The delay metrics of our design is 360 ps. In order to read the transition at the output register, we simulated for 3.5 clock period, which is 1.260 ns.

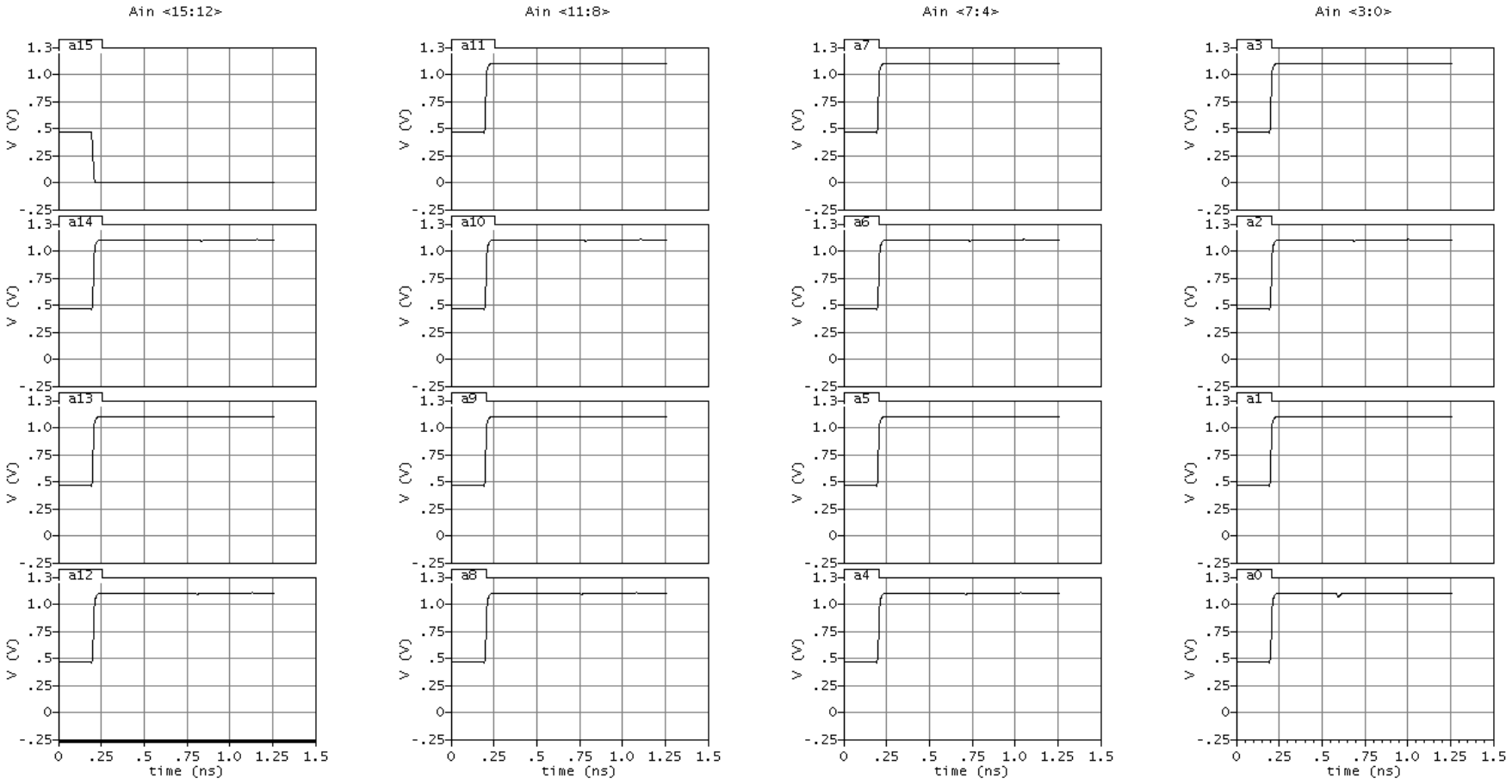

Figure 1 A_{in}<15:0>

Figure 1 and Figure 2 shows A_{in} and B_{in}, which are the latched output of input registers $regA$ and $regB$. Before first rising edge of the clock (0.18 ns), values of A_{in} and B_{in} are invalid. After the first rising clock edge $A_{in} = 0x7\text{FFF}$, and $B_{in} = 0x0000$. A_{in} then stays the same while B_{in} becomes $0x0001$ after the second rising edge (0.54 ns).

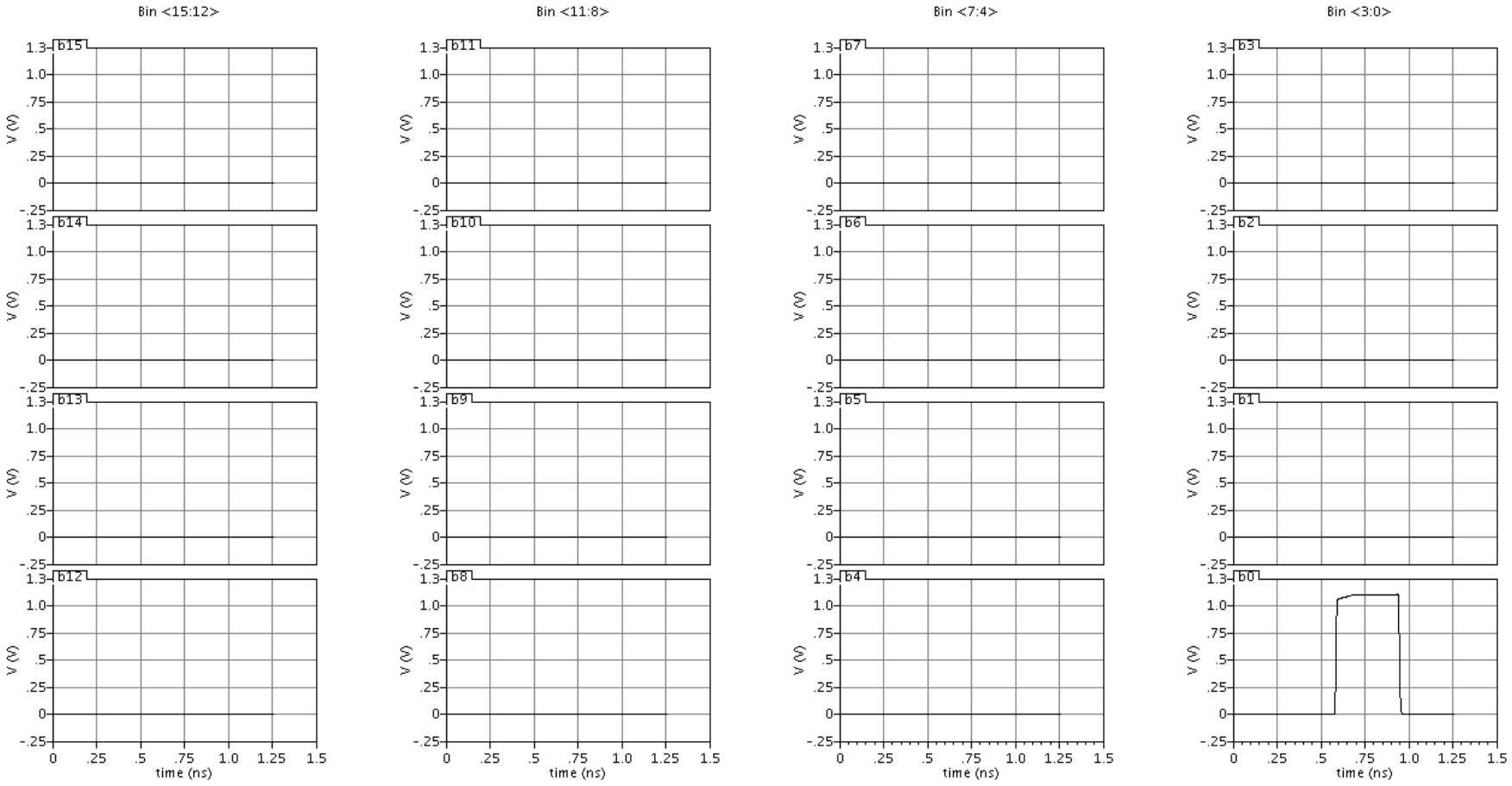

Figure 2 B_{in}<15:0>

Figure 3 shows $ALUout$, the unlatched ALU resulted selected by the ALU Mux. In the first cycle, it is expected to finally become to

$$ALUout = 0x7\text{FFF} + 0x0000 = 0x7\text{FFF}$$

In the second cycle, it is expected to finally become to

$$ALUout = 0x7\text{FFF} + 0x0001 = 0x8000$$

Figure 3 shows that Bit 15 transit from 0 to 1 while the other bits transit from 1 to 0, verifying the result.

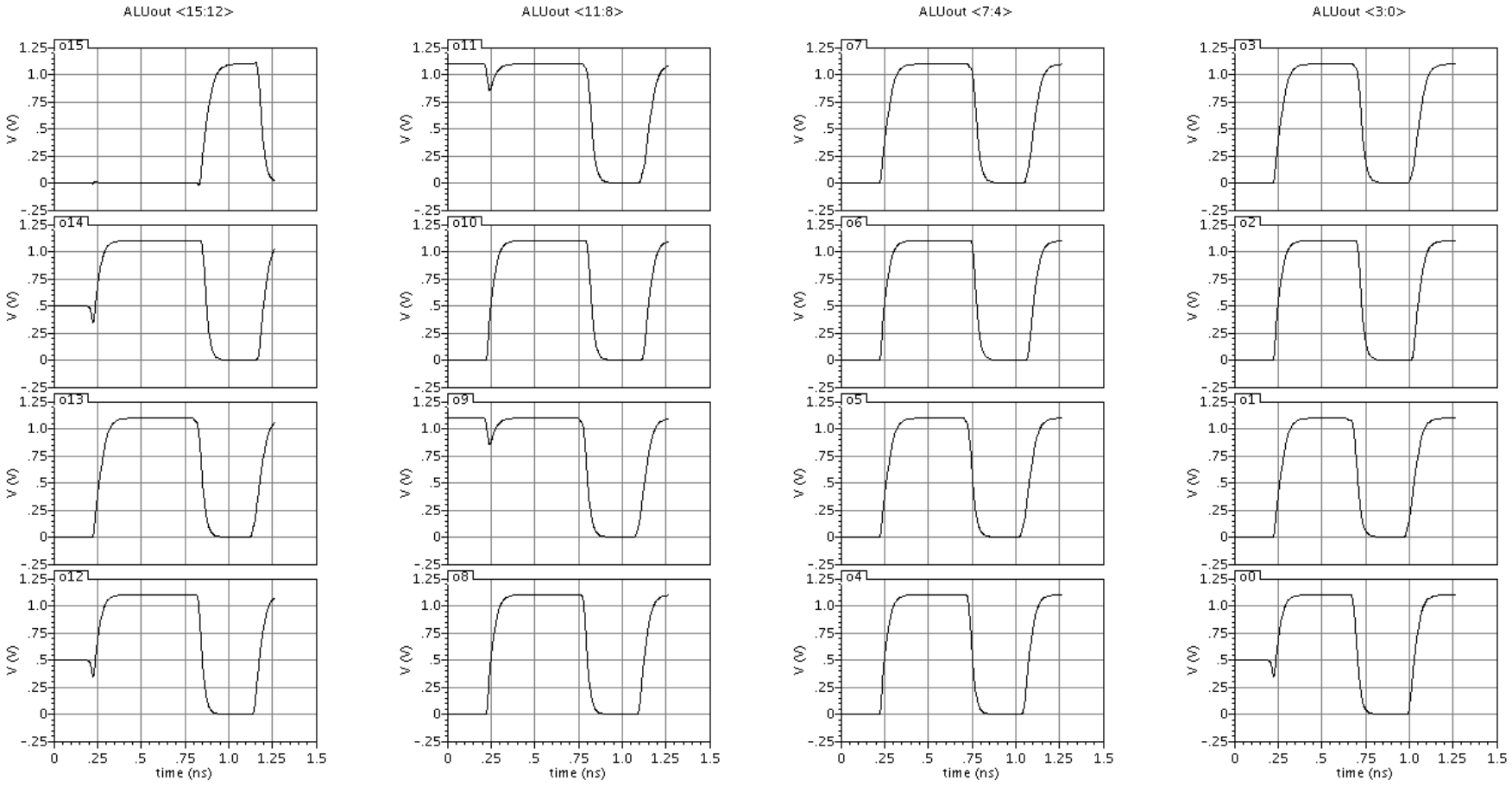

Figure 3 $ALUOut$<15:0>

Figure 4 and Figure 5 shows Out, register-latched result of $ALUOut$ signal, along with the clock signal. This is the final output of the DSP system. Final value of $ALUOut$ in the first clock cycle ($0x7FFF$) is expected to stay on Out during the second clock cycle, while the final value of $ALUout$ in the second clock cycle is expected to stay on Out during the third clock cycle. Both two plots match the expectation.

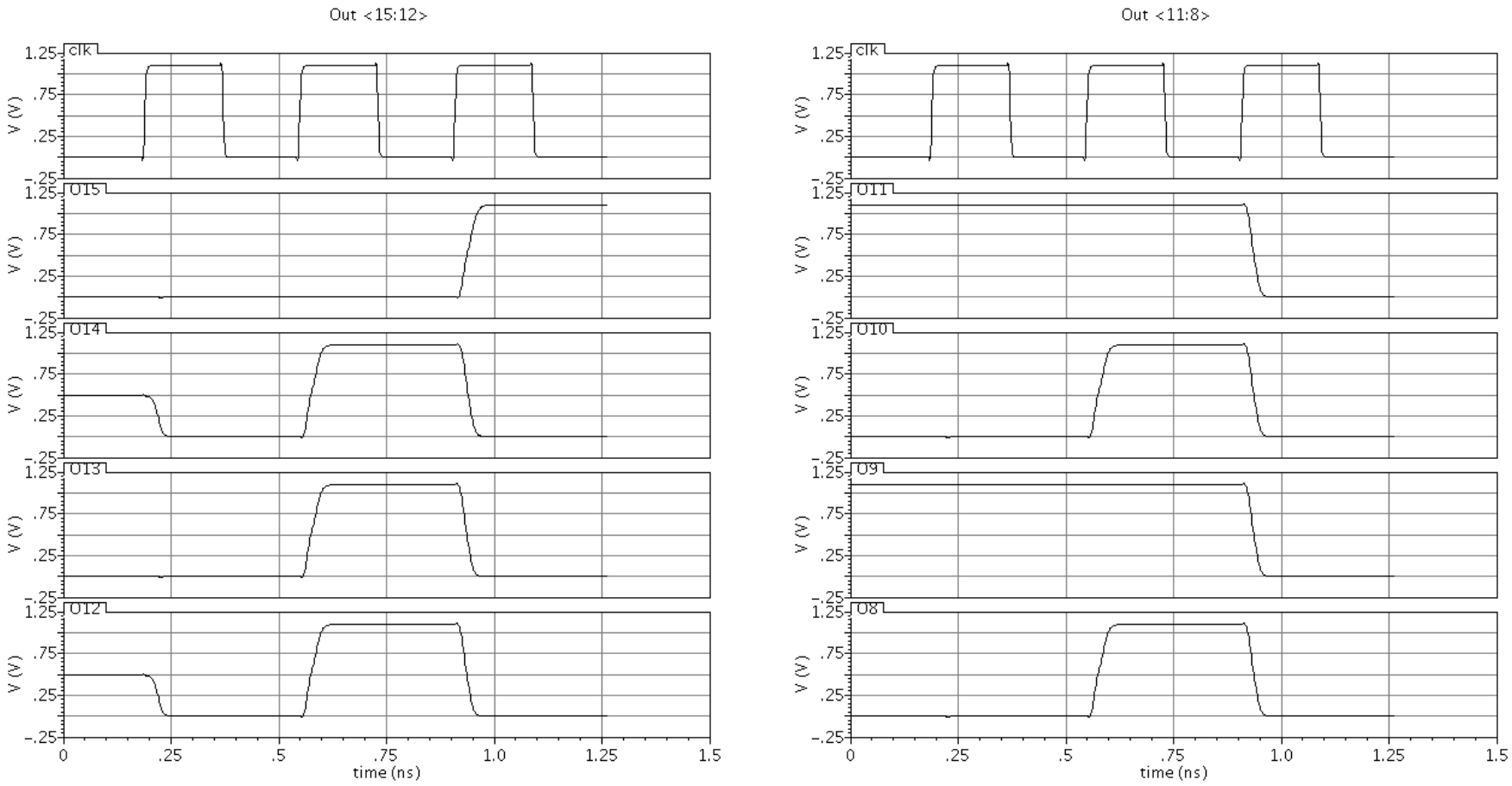

Figure 4 Out<15:8> and clk

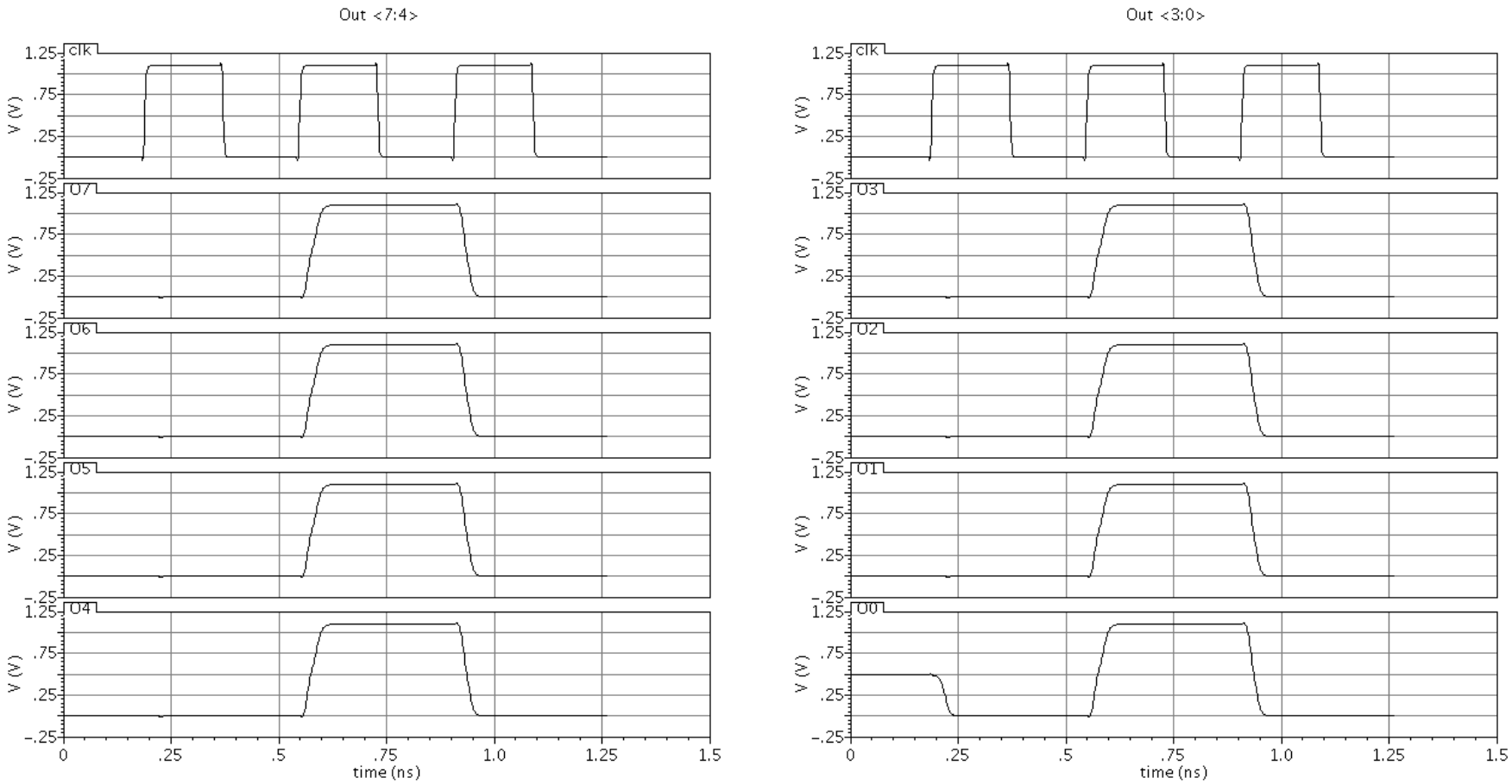

Figure 5 *Out*<7:0> and *clk*

Figure 6 shows the CarryOut signal of the ALU. In our worst case scenario, the sum at Bit 15 changes from 0 to 1 while the carry-out stays at 0. Therefore, it should be 0 (but some ripple in voltage maybe possible since it is not latched) during the simulation period.

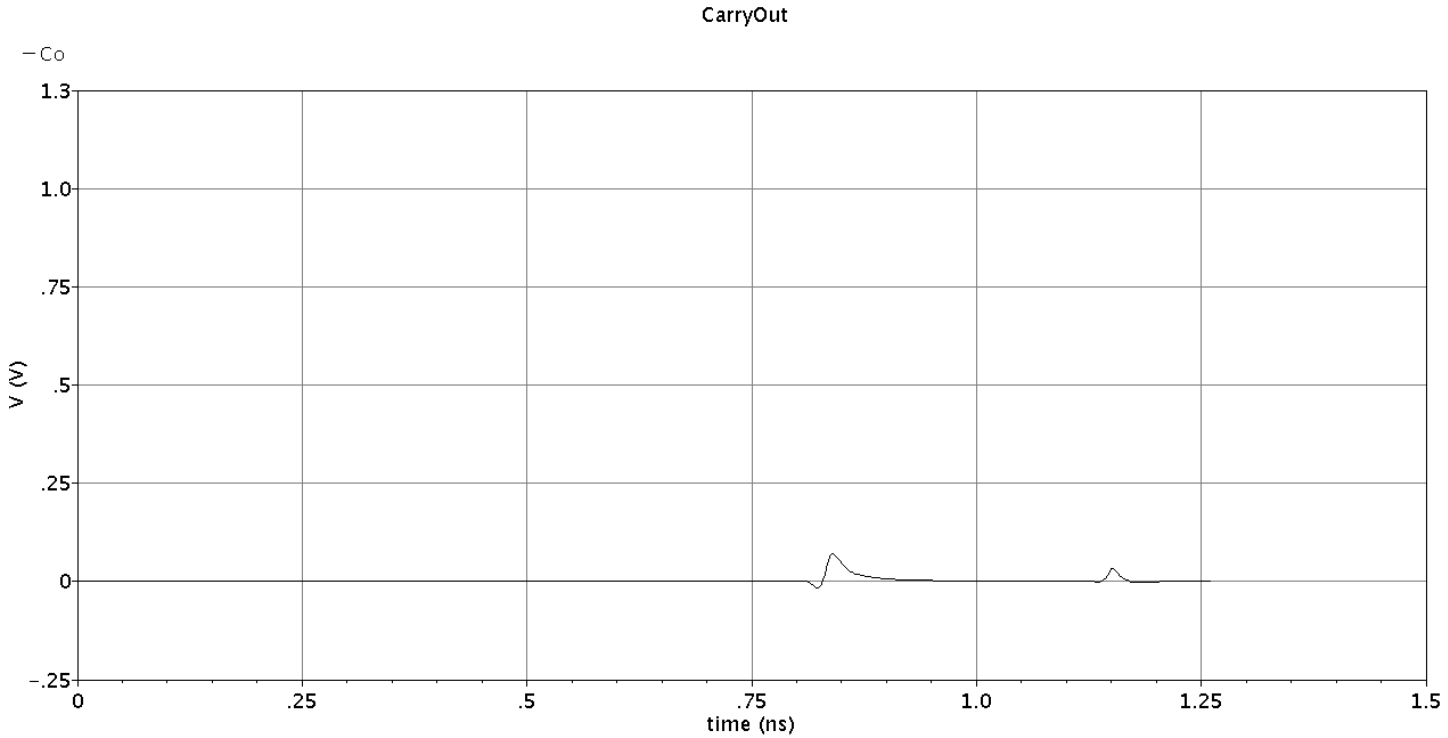

Figure 6 CarryOut

Simulation – Arbitrary Function

The purpose of this simulation is to verify the correctness of the arbitrary function. The arbitrary function in our design is a 8×8 multiplier. The ALU treats the lower 8 bits of both inputs as unsigned integers and calculate their product, as a 16-bit value.

Simulation – Energy Setup

This simulation is used to verify the correctness of all the basic functions, as the setup of energy simulation covers all basic functions, and some with different input values.

Figure 7 A_{in}<9:6>

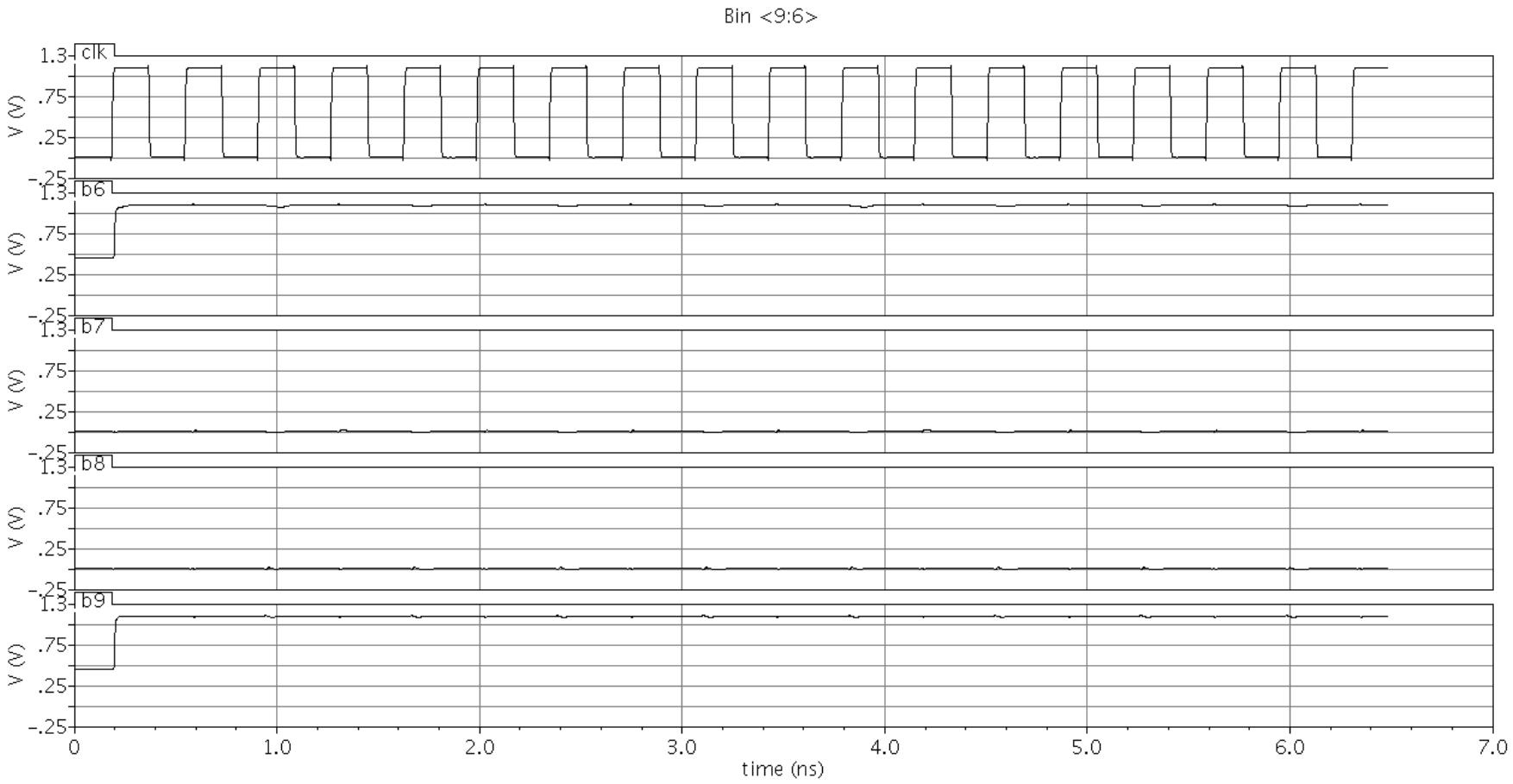

Figure 8 B_{in} <6:9>

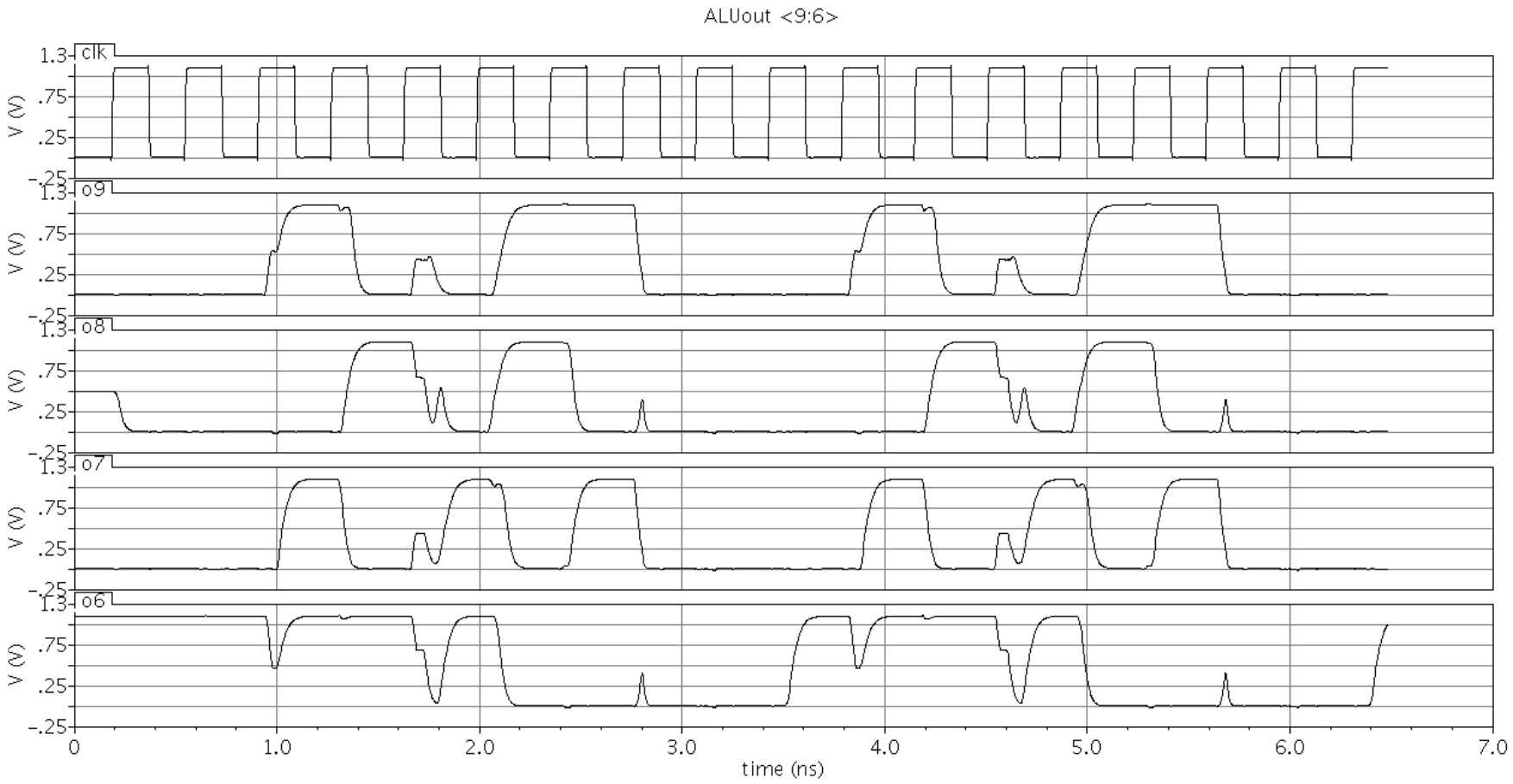

Figure 9 *ALUOut*<6:9>

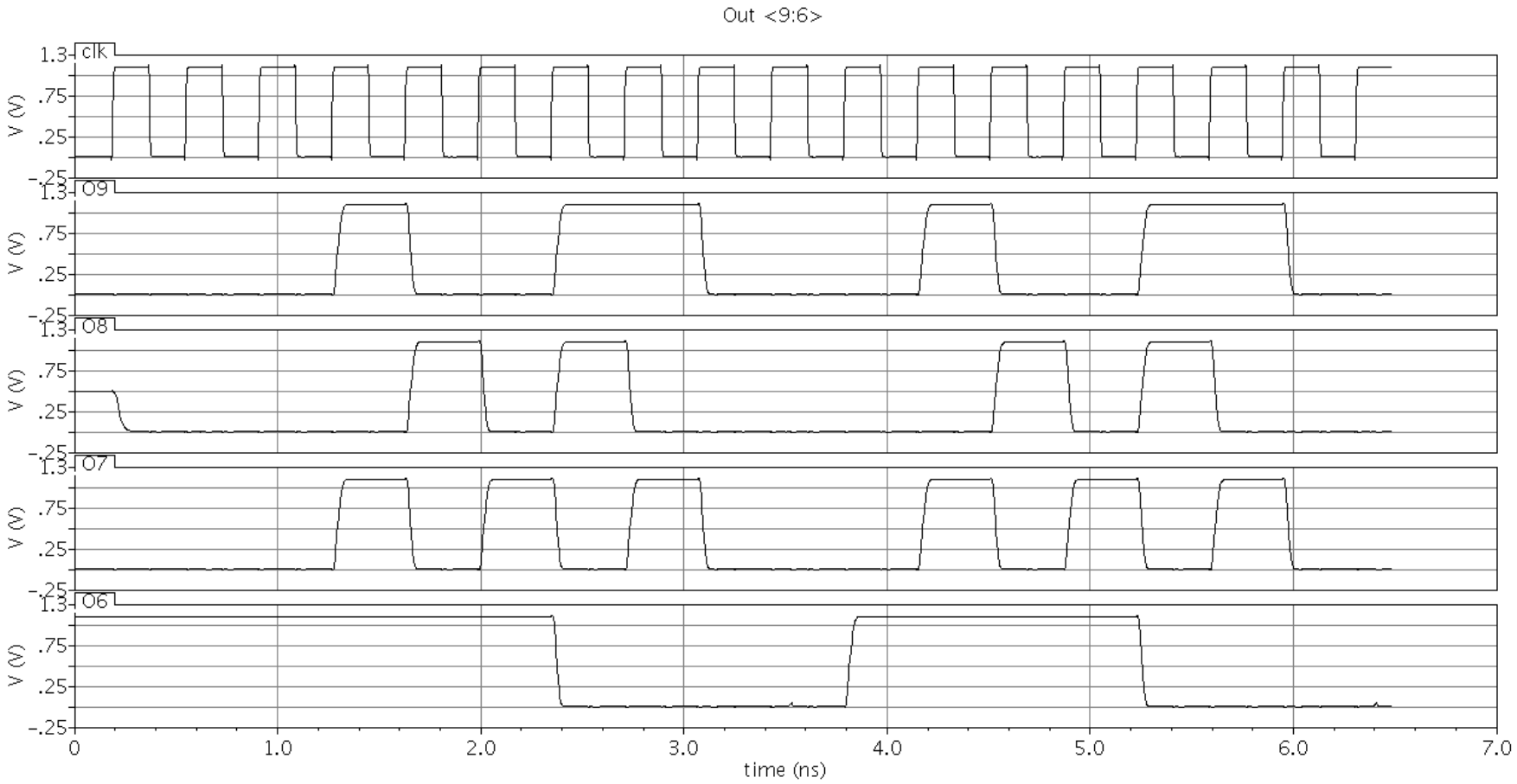

Figure 10 *Out*<6:9>

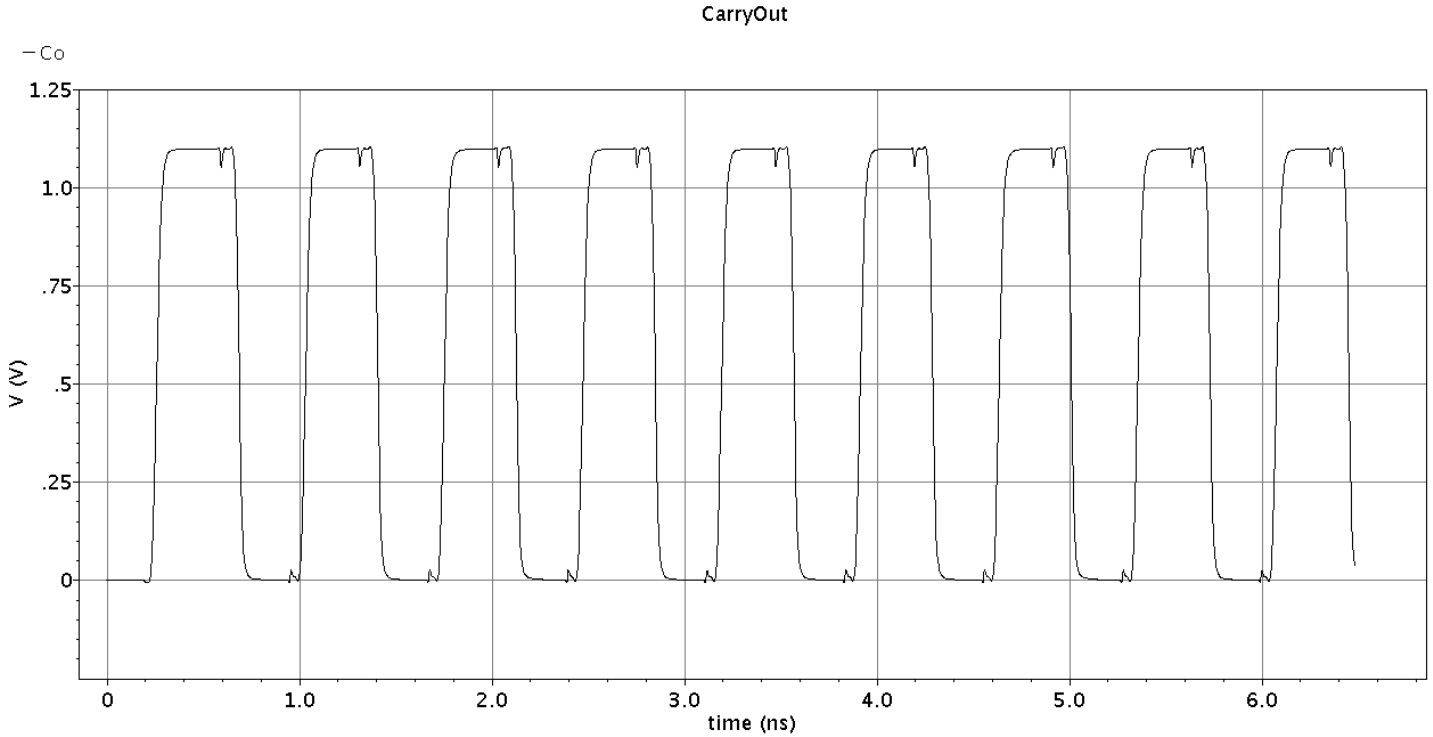

Figure 11 CarryOut

Expectation of the signals is shown in the following table. The Out column shows the expected output of the particular operation, which should appear on $ALUOut$ at the end of current stage, and on Out during the next clock period. B_{in} should always stays at $0x$AA55.

CarryOut is directly connected to the carry-out signal of the adder, which is meaningful when either addition or subtraction is selected, but it is nevertheless generated for every cycle. When $s_0 = 0$, addition is activated, and $0x\text{AAAA} + 0x\text{AA55} = 0x154\text{FF}$, resulting a "1" on the carry-out. When s_1, subtraction is activated, and $0x5555 - 0xAA55 = 0x\text{AB00}$, resulting "0" carry-out.

Table 1 Expected Signal Value

Cycle No.	s	A	Operation	Out
1	000	1010 1010 1010 1010	NOP	Invalid
9	000	1010 1010 1010 1010	NOP	0000 0000 0000 0000
2, 10	001	0101 0101 0101 0101	AND	0000 0000 0101 0101
3, 11	010	1010 1010 1010 1010	OR	1010 1010 1111 1111
4, 12	011	0101 0101 0101 0101	PASS	0101 0101 0101 0101
5, 13	100	1010 1010 1010 1010	AND	0101 0101 1111 1111
6, 14	101	0101 0101 0101 0101	SUB	1010 1011 0000 0000
7, 15	110	1010 1010 1010 1010	SHIFT	1010 1010 1010 1000
8, 16	111	0101 0101 0101 0101	Ground	0000 0000 0000 0000